A Versatile Pulse-Mode Biomimic Artificial Neuron Using A Capacitor-Free Integrate and – Fire Technique

Bruce C. Barnes and Richard B. Wells, Senior Member

Authors' affiliations:

Bruce C. Barnes and Richard B. Wells are with the MRC Institute, University of Idaho, BEL 317, Moscow, Idaho, USA, 83844-1024

Email address of corresponding author: wellsrb@ieee.org

A Versatile Pulse-Mode Biomimic Artificial Neuron Using A Capacitor-Free Integrate and – Fire Technique

Bruce C. Barnes and Richard B. Wells, Senior Member

Abstract - **A biomimic artificial neuron design with Schmitt trigger action potential pulsed outputs, independent excitatory and inhibitory pulsed inputs, and modulatory pulse width control is presented. The neuron is suitable for use in pulse-coded neural network applications.**

I. Introduction

Excitatory and inhibitory ionotropic inputs in a biological neuron [1] produce different levels of integrator responses depending on its operating state [2]. It is also known that action potential (AP) pulse width can be modulated by metabotropic synaptic inputs [1] in a variety of ways, and this affects postsynaptic response [3]. These are factors that provide the neuron with a greater information processing capacity than is generally incorporated into generic connectionist neuron models.

In previous reports [4], [5] we demonstrated the design of a non-linear, capacitor-free leaky integrator (LI). The differing rise and fall times of the LI and the capability of controlling the slower fall time via the gate voltages of non-linear input and feedback resistors (NLR s) formed from triode-region-biased PMOS transistors have been utilized to design an integrate-and-fire biomimic artificial neuron (BAN). We apply the output of the LI to a Schmitt trigger/inverter (ST/I) circuit. The high threshold output state of the ST/I constitutes the action potential of the neuron. The AP output disables excitatory current to the excitatory summing resistor (ESR) of the LI input, and switches the NLR gate voltages to obtain a fast fall time during LI discharge. This results in repolarization of the LI until the low threshold ST/I trigger is reached (1.83 volts for this design), and the AP pulse is ended. Integration can then resume until the high threshold trigger level (2.65 volts for this design) is reached and the cycle repeats. Higher average input current levels result in higher AP pulse repetition rates. Thus the average excitatory input current level is frequency modulated by the neuron.

The AP pulse width is modulated by controlling the gate voltage level of the NLR transistors during the AP output pulse. A higher NLR gate voltage results in a slower fall time of the LI [4], effectively delaying the time to reach the ST/I low threshold trigger level. The repolarization fall time is controlled by a clamping voltage (Vclamp) in the gate voltage subcircuit. A series PMOS transistor in the feedback path of the inverted AP output (M23 in Fig. 1) controls the LI time constant during integration. When the gate of the feedback path transistor is at ground the maximum available voltage is applied to the NRL gate voltage circuit, yielding low LI leakage during integration. If the gate of the transistor is lifted above ground the gate voltage of the NLR transistors is reduced, resulting in higher leakage for the LI. When the gate of M23 is greater than +4V, the feedback voltage is cut off, and the leakage during integration equals that of repolarization.

We have utilized this control capability to implement inhibitory synapses. An inhibitory pulse input diverts a portion of the ESR bias current to a second (inhibitory) summing resistor (ISR). The ISR voltage raises the gate voltage of M23, decreasing the LI time constant during an inhibitory input. This allows inhibitory pulses to pull the LI output lower and hence acts to inhibit firing the ST/I. In addition, we have implemented an AP pulse-width modulation control by switching Vclamp between two levels via an unclocked JK flip flop. This provides the BAN with an ability to mimic binary metabotropic modulatory input effects. Extension to m-ary modulation is straightforward.

II. Circuit

A schematic of the circuit is shown in Figure 1. The JK flip flop circuit is standard, and its details are omitted for brevity. Synaptic input weights are the current levels from transistor current mirrors M_{exc} and M_{inh}, and therefore the W/L ratios are application-dependent. The current mirror bias circuit is a standard design and thus is not shown. Switch transistors, M_{s1} and M_{s2}, have W/Ls that are application-dependant; for this design they are set to 5/2. The two MC transistors represent layout capacitances in the excitatory and inhibitory current paths. Table 1 lists the W/L ratios in μm for all the transistors in the circuit. All NMOS bodies are tied to ground, and all PMOS bodies are tied to +5V. The bias voltage circuits for M3, M4 and M11 are standard and are not shown. The total bias and excitatory input current flows through the ESR M4. The diverted inhibitory current flows through the ISR M3. The resulting voltages are level-translated by the source follower buffer circuits formed by M5/M6 and M31/M32 for

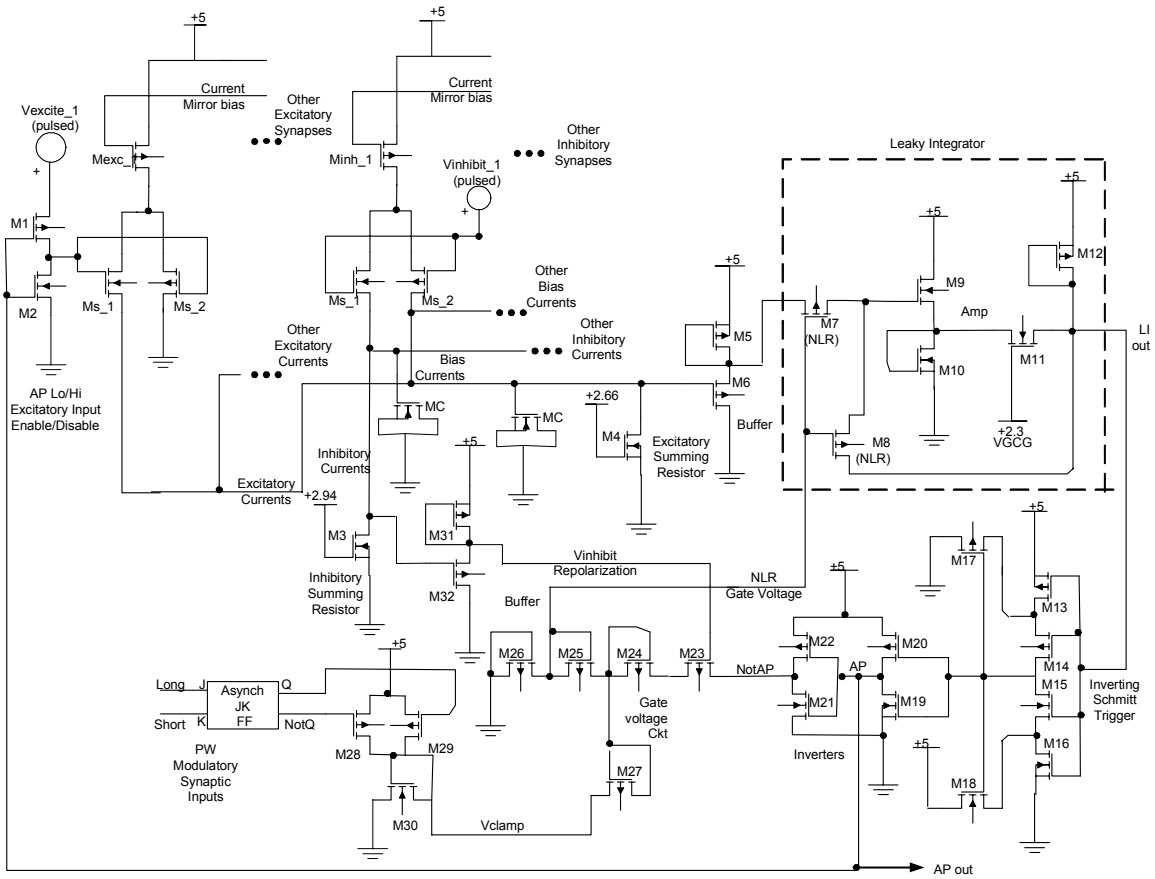

Figure 1: The Biomimic Artificial Neuron circuit. The leaky integrator core of the circuit appears in the dashed border. Synaptic excitatory and inhibitory inputs switch currents in and out of the summing resistor transistors. Modulatory synaptic inputs control the states of the JK flip flop. Devices sizes and functions are given in Table 1.

Table I
W/L RATIOS FOR CMOS TRANSISTORS

Synaptic Weight Current Mirrors Mexc and Minh: Application-dependent
Parasitic Capacitance Representations: MC: 20/20
Summing Resistors: M3: 5/10, M4: 5/2
Buffers: M5 & M6: 4/4, M31: 4/20, M32: 4/6
LI NLR s: M7: 4/4; M8: 4/20
LI Amplifier: M9: 8/2; M10: 20/2; M11: 20/2; M12: 4/5
Inverting Schmitt: M13: 4/4; M14-M16: 4/8; M17: 4/20; M18: 4/14
Inverters: M19-M22: 4/2.67
Gate Voltage Bias Circuit: M23: 4/4, M24, M25 & M27: 4/2; M26: 4/3
Vclamp Circuit: M28: 4/2, M29: 4/3, M30: 4/25
Switch Transistors: M_{s1} & M_{s2}: 5/2 (Application-dependant)
M1, M2: 4/2

excitatory and inhibitory cases, respectively. The buffered excitatory voltage is applied to the input NLR of the LI at the source of M7. The output of the LI at the drain of M11 goes to the ST/I circuit input. The AP output of the ST/I is fed to the gates of M1 and M2, which is the excitatory input enable/disable switch, cutting off the synaptic input signal while diverting the excitatory input currents to ground during AP firing. The inverted AP output (NotAP) is fed to the gate voltage circuit at the source of M23. The NLR gate voltage at the source of M26 is controlled by the combination of the gate voltage of M23 and the level of Vclamp. The voltage at the gate of M23 is governed by the buffered ISR voltage at the source of M32. Without an inhibitory input it is around 2.2 volts, and with inhibitory inputs it is lifted above that to a

maximum of about 4 volts, depending upon the total diverted inhibitory current. The voltage at Vclamp is determined by the switching of M28 and M29, changing the voltage divider ratio with M30. The output states, Q and NotQ, of the JK flip flop define the switching of M28 and M29. The pulsed J and K inputs provide for metabotropic pulse-width-modulation synaptic inputs, defined here as "long" and "short."

The excitatory and bias current sources are gated by the input switches, which are activated by excitatory or inhibitory AP inputs. Input pulses are active-high. The bias current is always present, and it is formed from the sum of the inhibitory synapse current sources. Inhibitory pulses divert bias current to the ISR, M3, when the inhibitory input AP is high.

The AP output voltage of the neuron is inverted prior to being applied to the gate voltage circuit at the source of M23. When the AP output is low the source of M23 is at +5 volts, and when the AP output is high the source of M23 is at ground. When the gate of M23 is at ground, the PMOS resistance is minimal and the maximum voltage available at the source of M23 is applied to the source of M24. While the AP output is low this results in about 1.96 volts being applied to the NLR gates via the source of M26, which yields the maximum decay time constant of the LI during integration.

All excitatory current is diverted to ground when the AP fires. With the neuron AP output high and excitatory inputs disabled, the source of M23 is at ground, causing the gate voltage circuit output at the source of M26 to drop to a level dependant upon the voltage Vclamp at the source of M27. This reduces the decay time constant of the LI. The speed of the LI fall time when M23 is cut off is governed by the voltage Vclamp at the source of M27. A lower Vclamp yields a faster fall time during repolarization (AP high) and a narrower AP. Raising Vclamp results in longer repolarization times, hence a wider output AP.

Changing the gate voltage of M23 varies the speed of the decay fall time of the LI. M23 is effectively cut off by a gate voltage of +4V or higher, which speeds up the fall time of the LI to the rate governed by Vclamp. The inhibitory current summed at the ISR, M3, produces the control voltage for M23. When an inhibitory pulse diverts current to the ISR, the LI fall time is shortened, effectively yanking the signal down in response to the inhibitory input.

For this BAN we have included a two-state setting of Vclamp via the asynchronous JK flip flop. Realization of a larger number of AP pulse widths is straightforward.

III. Results

Figure 2 shows how the output pulse repetition rate increases with excitatory input current steps of 5μA over the input level range of 100μA to 110μA dc with a bias current level of 80μA dc. Each input current increment (at 5μs and 7.8μs) increases the AP firing rate. The AP pulse width is about 450ns.

Figure 3 graphs the frequency vs. current level over the 100μA to 122μA dc range, in 2μA increments, with a bias level of 80μA dc. Not shown are the lower limit, which is where ST/I firing thresholds are not achieved, and the upper limit, where re-firing is instantaneous upon the ending of the AP. Within the range shown the curve demonstrates a sigmoid transfer characteristic. Midband gain is 140kHz/μA.

Figure 4 shows how AP output pulses are pulse-width-modulated by changing Vclamp. The repolarization fall time is varied due to the variation of Vclamp from 4.3 to 4.6 volts in steps of 0.1 volts at 6, 14, and 24 μs, respectively. Longer and shorter fall times exist beyond this range of Vclamp, but are not shown here. The NLR gate voltage during integration is set at 1.96 volts, resulting in a fixed LI risetime of 1.74 μs between APs at the input current levels used here. This is shown by the rising voltage of the LI output from the lower ST/I threshold of 1.83 volts toward the upper threshold of 2.65 volts. I_{bias} is at 80μA dc, and I_{exc} is at 95μA dc. Vclamp and the NLR gate voltages are shown on the plot.

Figure 5 shows the output pulse width increase on a logarithmic scale versus settings of Vclamp. The curve exhibits a monotonic parabolic shape, indicative of a well-behaved pulse-width modulation transfer characteristic. Within narrow operating ranges the curve is almost linear on a logarithmic scale, exhibiting an exponential response in those voltage ranges

Figure 6 illustrates the effect of inhibitory inputs for the cases where the inhibition follows an excitatory input pulse and the case where it precedes an excitatory input pulse. The figure illustrates the case where the sum-total of the excitatory inputs is 60 μA and the sum-total of the inhibitory inputs is 40 μA. The figure also illustrates what the excitatory response would have been if inhibition had not occurred (dashed line

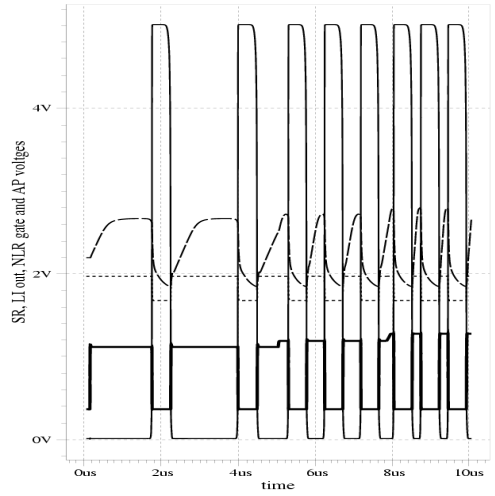

Figure 2: Pulse repetition rate increase of APs (____) with increased dc excitatory input currents (___). The LI output (_ _ _) reaches ST/I high threshold sooner for higher excitatory levels, while repolarization time to decay to ST/I low threshold is fixed. Vclamp is set at 4.2 volts, yielding an AP of around 450 ns. NLR gate voltage (……) is switched between integration and repolarization levels.

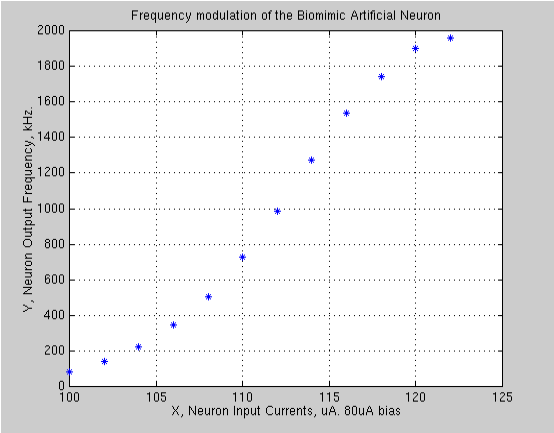

Figure 3: Frequency versus dc excitatory current. Ibias is at 80μA.

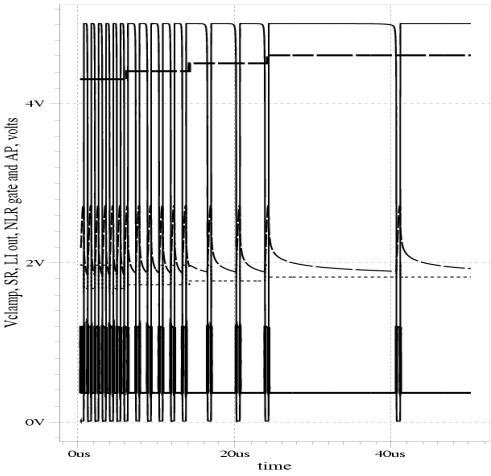

Figure 4: Pulse-width increase of the AP output (___) with time as the setting of Vclamp (----) is stepped in increments of 0.1 volts from 4.3 to 4.6 volts. NLR gate voltage (....) follows the Vclamp steps, and LI output fall times extend with each step.

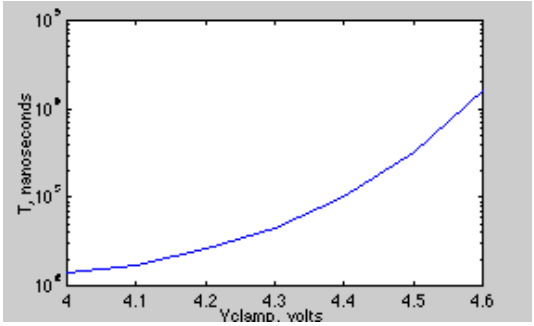

Figure 5: Pulse-width versus Vclamp.

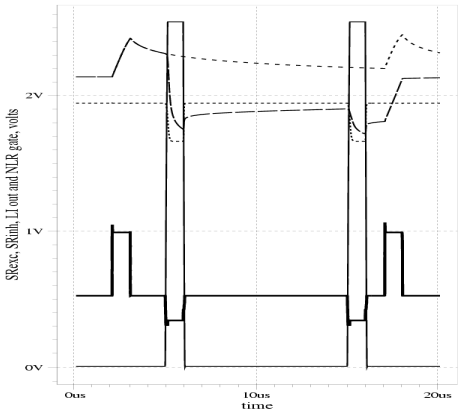

Figure 6: Inhibitory influence on LI output (_ _) during integration. The figure also illustrates what the LI output would have been if no inhibitory input had occurred (….). The ESR voltage curve (_____) shows the positive 60 μA excitatory and negative 40 μA inhibitory pulses on the bias level of 70 μA. The ISR voltage (_____) is much larger than that of the excitatory SR by design since this signal must control M23.

at the top of the figure). Comparing this response with that when inhibitory inputs are present, the effect of reducing the LI time constant due to inhibition is easily seen. These results are consistent with the effect of inhibitory inputs on membrane voltage in real neurons [2].

The ESR response shown in Figure 6 is disproportionately higher for the positive-going ESR pulses (i.e. excitatory pulses) than for the negative-going (inhibitory) pulses. This is because the ESR transistor is coming out of the triode region under the conditions illustrated in this example. The ISR response is much larger because of the design of M3 and its gate bias setting. This is done to put the buffered control signals (not shown) at the gate of M23 into the desired 2 to 4 volt range.

Other simulations under conditions where the inhibitory inputs are not sufficient to prevent the firing of action potentials (in response to a train of excitatory inputs) reveal that one of the principal effects of inhibition under these conditions is to modulate the firing time of the AP. This constitutes a form of pulse-position modulation of excitatory inputs by inhibitory inputs. Hence, the neuron is able to "encode" fairly complex information within the waveform by means of variations in inter-spike intervals. Hence, this neuron is capable of all three major non-amplitude encoding methods (i.e. pulse width modulation, pulse frequency modulation, and pulse phase modulation) available to pulse-stream neural networks [6].

IV. Discussion

Even a casual examination of Figure 1 shows that our neuron, although it is by no means an unusually complicated circuit, is electronically more complex than a number of simpler designs based on biomimetic analogies with the well-

known Hodgkin-Huxley axon model. Representative neurons of this class have been reported in, e.g., [7] and elsewhere. On the other hand, the majority of analog VLSI neuron designs reported in the literature employ one or more discrete capacitors in their designs. In those cases where capacitor values are reported, typical capacitor values seem to lie in the range from about 1 pF, e.g. [8] – [9], to tens of pF, e.g. [10]. Other designs are able to employ the much smaller FET gate capacitances but at the cost of introducing additional switching circuits and the associated clocking circuitry required to obtain "DRAM-like" charge storage. In some reported designs these neuron implementations show a complexity equal to or greater than the one we report here. Since capacitors are expensive in terms of chip area, the superiority of one design compared against another is likely to be application dependent. The neuron we report here repays the transistor design investment with flexibility in the signal processing operations it is able to perform.

The design we report here has fixed-value synaptic weights. In some applications of pulse-coded neural networks this is not disadvantageous, e.g. [11]. In other cases having an ability to adjust or adapt the synaptic weights would have clear advantages. We note here that incorporation of variable synaptic weights can be achieved in a number of ways, perhaps the simplest of which is a method reported by Liu and Frenzel [12].

We have shown that the properties of the capacitor-free LI can be utilized to mimic many of the basic behaviors of a biological neuron. The capability of controlling the fall time of the LI by the NLR gate voltage during the various states of the synaptic inputs and AP outputs in this design demonstrates great versatility of the LI circuit. The achievement of excitation, inhibition, integration, AP firing and repolarization, as well as modulatory control over all these biological neuron behaviors, was accomplished with relatively simple all-CMOS circuitry and no integrated passive components. Biological neurons number in the tens of thousands of specialized classes, but all are evolved from a basic biological foundation [13]. This basic BAN circuit lends itself to such a variety of classes.

Acknowledgement: This work was supported by the NSF-Idaho EPSCoR Program and by the National Science Foundation under award number EPS-0132626.

V. References

1. Wells, R.B., "Modulation channels in biomimic artificial neurons," *Proc. 28th Ann. Conf. Ind. Electronics* (IECON02), Nov. 5-8, 2002, Sevilla, Spain, pp. 3209-3214.
2. Shepherd, G., *Neurobiology*, 3rd ed., N.Y.: Oxford University Press, 1994.
3. Levitan, I. B. and Kaczmarek, L. K., "Neuromodulation: Mechanisms of Induced Changes in the Electrical Behavior of Nerve Cells," *The Neuron: Cell and Molecular Biology*, N.Y.: Oxford University Press, 2002.
4. Wells, R. B., and Barnes, B. C., "Capacitor-free leaky integrator for biomimic artificial neurons," *IEE Letters,* vol. 38, no. 17, 15th Aug., 2002, pp. 974-976.
5. Wells, R. B., and Barnes, B. C., "Delay-Resistor Implementation of Integrators in Biomimic Artificial Neurons," *Proc. 28th Ann. Conf. Ind. Electronics* (IECON '02), Nov., 2002, Seville, Spain, pp. 3186-3190.
6. Murray, A.F., Del Corso, D., and Tarassenko, L., "Pulse-stream VLSI neural networks mixing analog and digital techniques," *IEEE Trans. Neural Networks*, vol. 2, no. 2, Mar., 1991, pp. 193-204.
7. Ota, Y. and Wilamowski, B.M., "VLSI architecture for analog bidirectional pulse-coupled neural networks," *Proc. 1997 Intl. Conf. on Neural Networks* (ICNN '97), June 9-12, 1997, pp. 964-968.
8. Montalvo, A.J., Gyurcsik, R.S., and Paulos, J.J., "An analog VLSI neural network with on-chip perturbation learning," *IEEE J. Solid State Ckt.*, vol. 32, no. 4, Apr., 1997, pp. 535-543.
9. Heim, P. and Vitoz, E.A., "Precision analog synapse for Kohonen feature maps," *IEEE J. Solid State Ckt.*, vol. 29, no. 8, Aug., 1994, pp. 982-985.
10. Moon, G., Zaghioul, M., de Savigny, M., and Newcomb, R.W., "Analysis and operation of a neural-type cell (NTC), *Proc. IEEE ISCAS*, June, 1991, pp. 2332-2334.
11. Johnson, J.L. and Padgett, M.L., "PCNN models and applications," *IEEE Trans. Neural Networks*, vol. 10, no. 3, May, 1999, pp. 480-498.
12. Liu, B., and Frenzel, J.F., "A CMOS neuron for VLSI implementation of pulsed neural networks," *Proc. 28th Ann. Conf. Ind. Electronics* (IECON02), Nov. 5-8, 2002, Sevilla, Spain, pp. 3182-3185.
13. Kandel, E. R., "Nerve Cells and Behavior," in *Principles of Neural Science*, 3rd ed., E. R. Kandel, J. H. Schwartz, and T. M. Jessell (eds.), East Norwalk, CN: Appelton & Lange, 1991.