PWM Characteristics of a Capacitor-Free Integrate-and-Fire Neuron

Bruce C. Barnes, Richard B. Wells and James F. Frenzel

Authors' affiliations:

Bruce C. Barnes, Richard B. Wells and James F. Frenzel (MRC Institute, University of Idaho, BEL 317, Moscow, Idaho, USA, 83844-1024)

Email address of corresponding author: rwells@uidaho.edu

PWM Characteristics of a Capacitor-Free Integrate-and-Fire Neuron

Bruce C. Barnes, Richard B. Wells and James F. Frenzel

An artificial neuron with Schmitt trigger action potential pulsed outputs demonstrating pulse-width modulation capability is presented. One signal processing application of this capability is the mimicking of neuronal burst phenomena without the need for explicitly generating burst trains of individual pulses.

Introduction: The width of an output action potential (AP) of a biological neuron is often modulated by synaptic inputs [1][2][3]. In a previous report [4] we demonstrated the design a capacitor-free leaky integrator (LI) . Of particular importance in the LI were the differing rise and fall times of the integrator and the capability of controlling the slower fall time. The gate voltage of non-linear input and feedback resistors (NLRs), formed from triode-region-biased PMOS transistors, controls the fall time. We have applied the output of the LI to drive a Schmitt Trigger/Inverter (ST/I) circuit to implement an integrate-and-fire biomimic artificial neuron (BAN). Here we report on the capability of modulating the output AP pulse widths via a synaptic control.

The ST/I output represents the AP of the BAN. The ST/I high threshold output state is used to disable the excitatory current inputs to the summing resistor (SR) of the LI input, and to switch the NLR gate voltages to obtain fast repolarization of the LI circuit. The LI output falls until the low threshold ST/I trigger level is reached (1.83 volts for this

design), and the AP pulse is ended. For a dc level current input integration resumes until the high threshold trigger level is reached (2.65 volts for this design), and the ST/I fires again, repeating the cycle. The AP pulse-width is modulated by controlling a clamping voltage input, Vclamp, in the NLR gate voltage circuit. Decreases in Vclamp produce faster fall times during repolarization; increases in Vclamp produce slower fall times.

Circuit: A schematic of the circuit is shown in Figure 1. Transistor width/length ratios are given in Table 1.The test input current sources I_{exc} and I_{bias} are ideal. The NOR and Iswitch circuits are standard and are omitted for brevity. The bias current is always present, and the input current is switched in via the voltage-controlled switch. I_{exc} represents the normal synaptic input to the neuron, and Vclamp represents a modulatory input. The active-low controlling voltage of the switch is NOR'ed with the AP output, resulting in the disabling of the excitatory input signal with high AP output. The AP voltage is inverted (NotAP in the schematic) prior to being applied to the feedback voltage port of the gate voltage circuit at the source of M23. When the AP output is low the source of M23 is at +5 volts, resulting in about 1.96 volts being applied to the NLR gates via the source of M25. This produces a slow fall time in the LI during integration, hence good integration characteristics [4], [5]. When the AP is high the source of M23 is at ground and Vclamp limits the NLR gate voltage to a lower value, resulting in a faster fall time for repolarization. The repolarization time is modulated by varying Vclamp. Increasing Vclamp increases the NLR gate voltage during AP output, thereby increasing the time required to reach the low-level threshold of the ST/I and extending the AP pulse-width. The opposite effect is achieved by reducing Vclamp.

Results: Figure 2 shows AP output pulses which are pulse-width modulated by changing Vclamp. The repolarization fall time is varied due to the variation of Vclamp from 4.3 to 4.6 volts in steps of 0.1 volts at 6, 14, and 24 μs, respectively. Longer and shorter fall times exist beyond this range of Vclamp but are not shown here. The NLR gate voltage during integration is set at 1.96 volts, resulting in a fixed LI risetime of 1.74 μs between APs at the input current levels used here. I_{bias} is 80μA dc and I_{exc} is 95μA dc. This produces the rising voltage of the LI output from the lower ST/I threshold of 1.83 volts toward the upper threshold of 2.65 volts. Vclamp and the NLR gate voltages are shown on the plot. The NLR gate voltage is fixed during integration by the signal NotAP (5 volts). During AP output, NotAP is low, diode M26 is turned on, and the NLR gate voltage is determined by Vclamp and the voltage division circuit M24, M25, and M26.

Figure 3 shows the output pulse width vs. Vclamp on a logarithmic scale. The curve exhibits a monotonic parabolic shape, indicative of a well-behaved, high-sensitivity pulse-width modulation transfer characteristic. Within narrow operating ranges (< 100 mV) the curve is almost linear on a logarithmic scale, an exponential response to Vclamp. The characteristics of this curve provide for easy separation of *m*-ary valued modulations of Vclamp. The variety of pulse width obtainable through this modulation can be regarded as one means of mimicking neuronal bursting phenomena without the need to explicitly generate a burst of pulses in response to normal (non-modulatory) synaptic inputs.

Acknowledgement: This work was supported by the NSF-Idaho EPSCoR Program and by the National Science Foundation under award number EPS-0132626.

References

1. Grossburg, S. (1970), "Neural Pattern Discrimination," *Journal of Theoretical Biology,* vol. 27, 1970, pp. 291-337.
2. Rieke, F., Warland, D., de Ruyter van Steveninck, R., and Bialek, W.(1996). *Spikes – Exploring the Neural Code*. MIT Press, Cambridge, MA.
3. Levitan, I. B. and Kaczmarek, L. K. (2002), "Neuromodulation: Mechanisms of Induced Changes in the Electrical Behavior of Nerve Cells," Ch. 13, pp. 315-338 ,*The Neuron Cell and Molecular Biology,* Oxford University Press, New York, NY.
4. Wells, R. B., and Barnes, B. C., "Capacitor-free leaky integrator for biomimic artificial neurons," *IEE Letters, vol. 38, no. 17, 15th Aug., 2002.*
5. Wells, R. B., and Barnes, B. C., "Delay-Resistor Implementation of Integrators in Biomimic Artificial Neurons," *Proc. 28th Ann. Conf. Ind. Electronics (IECON '02), Nov., 2002, Seville, Spain, Pp. 3186-3190.*

Figure captions

Fig. 1 Biomimic Artificial Neuron circuit

Fig. 2 Biomimic Artificial Neuron output pulse widths controlled by DC clamping voltages, VCLAMP, from 4.0 to 4.6 volts in increments of 0.1v. Bias current is at 80μA, and input current is at 100μA..

Summing resistor voltage at drain of M4.

_ _ _ _ _ _ _ _ Leaky Integrator output voltage at drain of M11.

———————— Schmitt Trigger / Inverter AP output voltage.

_ _ _ _ _ _ _ _ _ _ NLR voltage at gates of M7 and M8.

▬ ▬ ▬ Vclamp Control voltage

Fig.3 Biomimic Artificial Neuron AP pulse width vs. controlling voltage, Vclamp.

Table Captions

Table 1 Transistor width to length ratios (μm/μm).

Authors' affiliations:

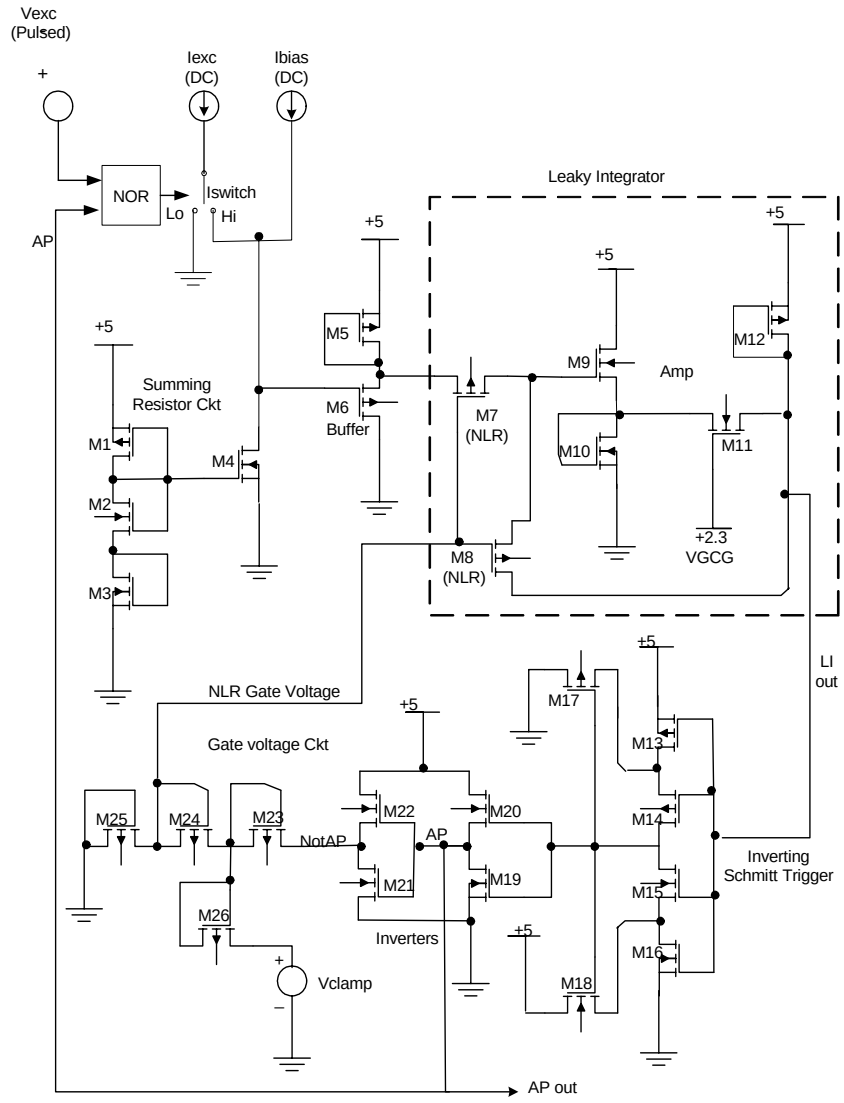
Bruce C. Barnes, Richard B. Wells and James F. Frenzel (MRC Institute, University of Idaho, BEL 317, Moscow, Idaho, USA, 83844-1024)

Email address of corresponding author: rwells@uidaho.edu

Table 1

Summing Resistor: M1-M4: 4/2; M4: 5/2 Buffer: M5 & M6: 4/4 LI NLRs: M7: 4/4; M8: 4/20 LI Amp: M9: 8/2; M10: 20/2; M11: 20/2; M12: 4/5 Inverting Schmitt: M13: 4/4; M14-M16: 4/8; M17: 4/20; M18: 4/14 Inverters: M19-M22: 4/2.67 Gate Voltage Bias Circuit: M23, M24, & M26: 4/2; M25: 4/3

Figure 1


Vexc
(Pulsed)
+
Iexc
(DC)
Ibias
(DC)
NOR
Iswitch
Lo
Hi
AP
+5
M5
M6
Buffer
Summing
Resistor Ckt
M1
M2
M3
M4
Leaky Integrator
M7
(NLR)
M8
(NLR)
M9
Amp
M10
M11
M12
+2.3
VGCG
LI
out
NLR Gate Voltage
Gate voltage Ckt
M17
M13
M14
M15
M16
M18
M19
M20
M21
M22
M23
M24
M25
M26
NotAP
Inverters
Inverting
Schmitt Trigger
Vclamp
AP out